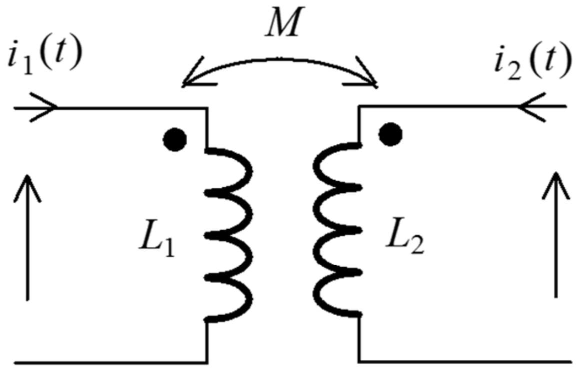
EG1108 Tutorial 5: Transformers & Rectifier Circuits – Part 1

1. It is shown in the lecture that an ideal mutual inductor has the following properties:

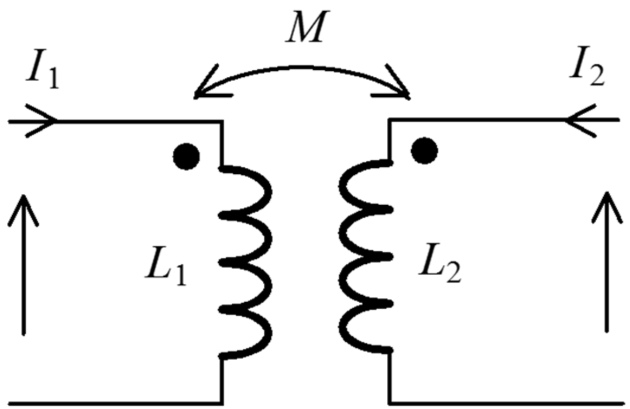


$$v_1(t) = L_1 \frac{di_1(t)}{dt} + M \frac{di_2(t)}{dt}$$

$$v_2(t) = M \frac{di_1(t)}{dt} + L_2 \frac{di_2(t)}{dt}$$

$$L_1 = \frac{N_1^2}{\mathfrak{R}}, \; L_2 = \frac{N_2^2}{\mathfrak{R}}, \; M^2 = L_1 L_2 \text{ for no flux leakage and perfect coupling}$$

Show in the AC environment, the properties can be represent in following phasor form:



$$V_1 = j\omega L_1 I_1 + j\omega M I_2$$

$$V_2 = j\omega M I_1 + j\omega L_2 I_2$$

EG1108 Tutorial 5 (cont.)

2. An ideal transformer has a turns ratio of 3:2. It is desired to operate a 200 Ω resistive load at 150 V. Find the primary and secondary currents, the source voltage, the power delivered to the primary from the source, and the impedance the source sees looking into the primary winding.

Answers: 0.5 A, 0.75 A, 225 V, 112.5 W, 450 Ω

3. A transformer is to be used to match an 8 Ω loudspeaker to a 500 Ω audio line. The audio power delivered to the speaker is 10W. Find:

   i. turns ratio of the transformer,

   ii. the voltages at primary and secondary terminals of the transformer.

   Assume that the speaker is resistive and that the transformer is ideal.

Answers: turns ratio = 7.9:1; V_2= 8.94 V, V_1 = 70.6V

4. The high voltage side of a step-down transformer has 800 turns, and the low voltage side has 100 turns. A voltage of $240\angle 0°$ V is applied to the high voltage side and a $3+j\,4$ Ω load is connected on the low voltage side. Find:

   i. The secondary voltage and current.

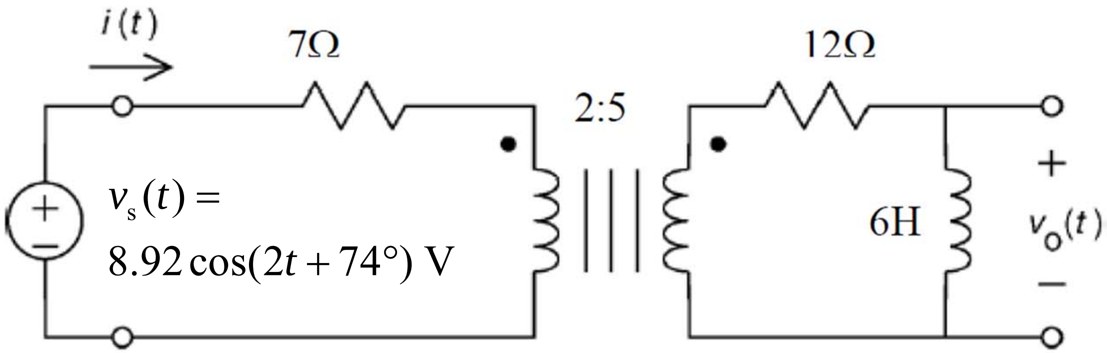
   ii. The primary current.

   iii. The reflected impedance seen from the primary side.

Answers: $30\angle 0°$ V, $6\angle -53.13°$ A; $0.75\angle -53.13°$ A; $320\angle 53.13°$ Ω

EG1108 Tutorial 5 (cont.)

5. Consider the transformer circuit as shown below. The input to the circuit is the voltage of the voltage source, $v_s(t)$. Determine the output voltage, $v_o(t)$ across the 6H inductor. The transformation ratio is 2:5.



Answer: $v_o(t) = 4.684\cos(2t + 151.85°)$ V

EG1108 Tutorial 6: Transformers & Rectifier Circuits – Part 2

1. i. A voltage source V_S is connected to a resistive load R_L = 10 Ω by a transmission line having a resistance R_{line} = 10 Ω, as shown in Figure Q1.1. Determine the power delivered by the source, power lost in the line resistance, power delivered to the load and the efficiency (expressed as the power delivered to the load as a percentage of power supplied by the source).

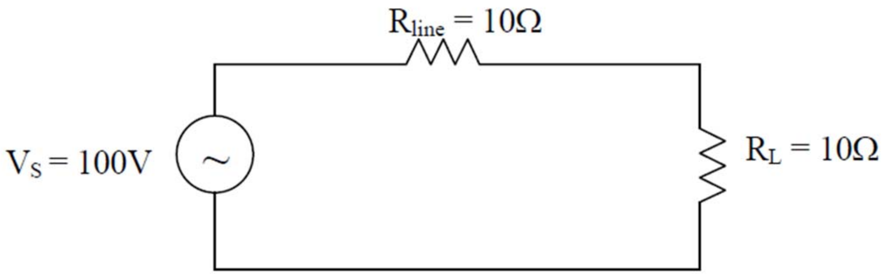


Figure Q1.1

ii. This power transmission system is now modified to include two transformers. A transformer of turns ratio 1:10 is used to step up the source voltage at one end of the transmission line (sending end), and another transformer of turns ratio 10:1 is used to step down the voltage to 100V at the load (receiving end) as shown in Figure Q1.2. Calculate the power delivered by the source, power lost in the line resistance, power delivered to the load and the efficiency in this case, and compare with the values obtained in (i) above. What conclusions can you draw from this?

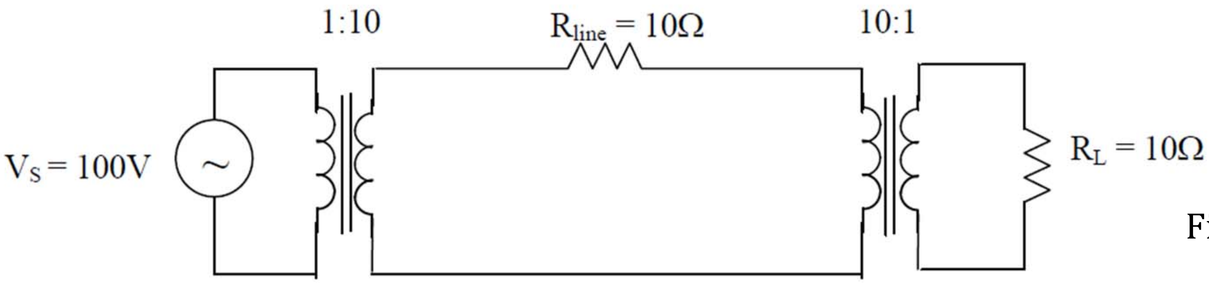


Figure Q1.2

Answers: i. Efficiency = 50%; ii. Efficiency = 99.01%

EG1108 Tutorial 6 (cont.)

2. A DC power supply consists of a transformer feeding a half-wave rectifier together with a capacitor filter. It supplies a DC current of 1A at 12V DC to an electronic equipment. The AC input source is 230V (rms) at 50Hz. The output side filter capacitor used is 50000μF.

   i. Draw the circuit diagram of the supply arrangement.

   ii. Determine a suitable winding ratio for the transformer. Treat the operation of the power supply as ideal (i.e., neglect voltage drop in the diode and assume that the transformer is ideal).

   iii. What is the peak-to-peak ripple in the output voltage? What is the ripple frequency? What is the percentage ripple?

   iv. Sketch the following waveforms: AC input voltage, secondary AC voltage, rectifier output voltage. Mark the interval when the diode conducts.

Answers: (ii) 27:1; (iii) % ripple = 3.33%

3. A full wave bridge rectifier, with a large smoothing capacitor is supplying power to a 10 Ω load resistance. The secondary voltage of the transformer supplying power the rectifier is 8 V (rms) at 50 Hz. Assuming that the diodes are ideal, what is the approximate value of filter capacitor required such that the peak-to-peak ripple is 5% or less?

Answer: 0.02 F

4. The rectifier supply shown in Figure Q4 is used as part of an electronic circuit. The input voltage is sinusoidal with a peak amplitude of 50V, and 10 kHz frequency. The transformer primary to secondary ratio = 1:3. The load resistance is 10kΩ. Neglect diode conduction voltage drops. Also, assume ideal operation of the transformer neglecting leakage, losses etc.

   i. Determine the output DC voltage. What is the peak-to-peak ripple in the output voltage? What is the percentage ripple?

   ii. Sketch waveforms for v_1, v_2, v_3, v_{YX}, v_o, i_o, i_2, i_3, v_{D2}. Mark the diode conduction intervals.

   iii. What is the maximum reverse voltage applied across the diodes? When do they occur?

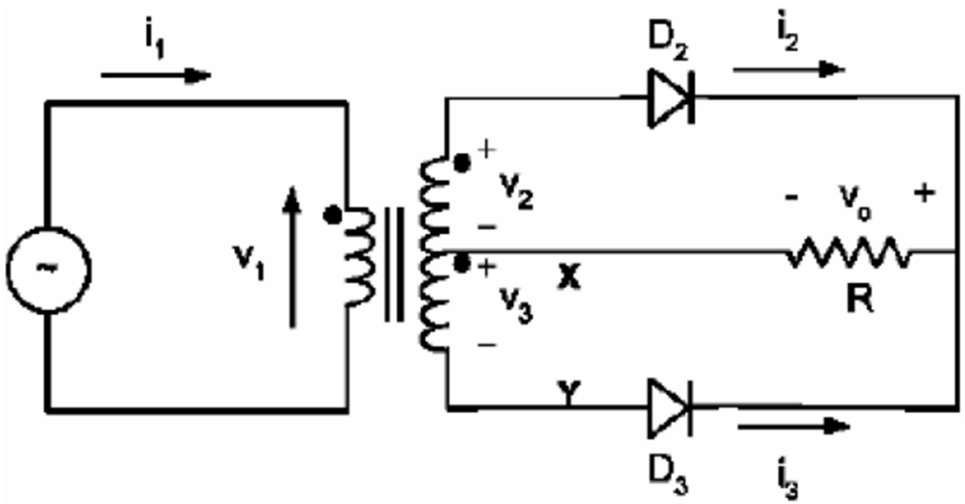
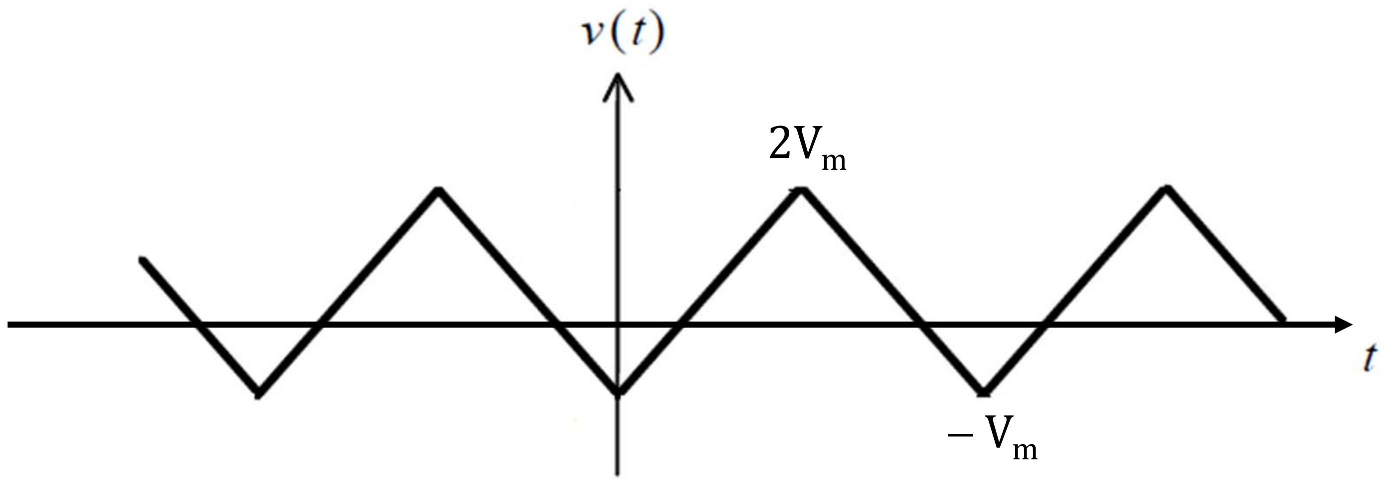


Figure Q4

Answers: i. 47.8V; 75V; 157%; iii. 150V

EG1108 Tutorial 6 (cont.)

5. For the half-wave and full-wave rectifier circuits with capacitor filtering that we have studied, comment whether the resulting output voltage will be smooth DC if the input voltage is given as follows.



Give your justification.

Answers: Yes if the capacitance is sufficiently large

EG1108 Tutorial 7: Digital Logic Circuits – Part 1

1. Simplify the following Boolean expressions using rules of Boolean Algebra and De Morgan's theorems:

   i. $F = (A+B)\cdot(A+\overline{B})$ Answer: $F = A$

   ii. $F = \overline{(\overline{A}+B)\cdot(\overline{C}+D)\cdot\overline{C}}$ Answer: $F = A\cdot\overline{B}+C$

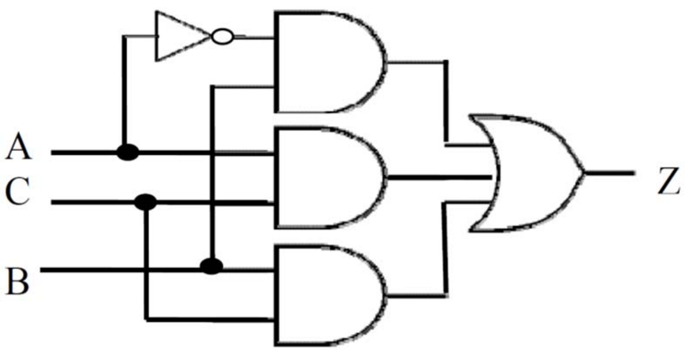
   iii. $F = A\cdot B\cdot C + A\cdot\overline{B}\cdot\overline{C} + \overline{A}\cdot\overline{C} + \overline{A}\cdot B\cdot\overline{D} + B\cdot\overline{C}$ Answer: $F = B\cdot(A+\overline{D})+\overline{C}$

   iv. $F = \overline{A+B} + A\cdot\overline{B} + B\cdot\overline{C}$ Answer: $F = \overline{B\cdot C}$

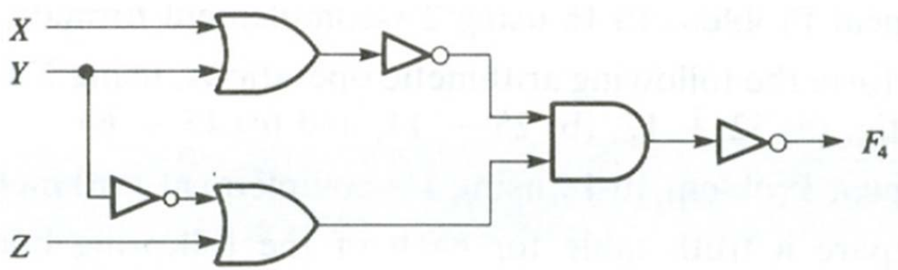
   v. $F = \overline{(A+B)\cdot\overline{(A+\overline{C})}\cdot(B+C)}$ Answer: $F = A+\overline{B}+\overline{C}$

2. Derive the Boolean functions for the combinatorial network shown in figures below.

i)



ii)



Answers: $Z = \overline{A}\cdot B + A\cdot C + B\cdot C$

$F_4 = \overline{(\overline{X+Y})\cdot(Z+\overline{Y})} = X+Y$

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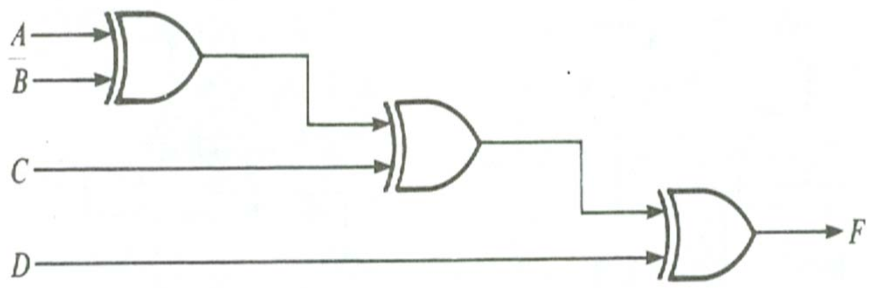
3. Use only NOR gates with 2 inputs to find a way to implement the exclusive OR function $Z = A \oplus B$.

4. Use only NAND gates with 2 inputs to find a way to implement the exclusive NOR function $Z = \overline{A \oplus B}$.

5. The logic circuit below is known as a parity checker for a 4-bit binary number.

   i. Construct a truth table for the circuit.

   ii. Verify that F is true if and only if the number of the inputs that are high is either 1 or 3.



EG1108 Tutorial 8: Digital Logic Circuits – Part 2

1. The truth table below shows the relationship between inputs A, B and C, and the output Z.

   i. Find Z in terms of A, B and C using Sum-Of-Products (SOP) form.

   ii. Find Z in terms of A, B and C using Product-Of-Sums (POS) form.

A	B	C	Z
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Answers: SOP: $Z = \overline{A}\cdot\overline{B}\cdot\overline{C} + \overline{A}\cdot\overline{B}\cdot C + \overline{A}\cdot B\cdot C + A\cdot\overline{B}\cdot C$

POS: $Z = \left(A+\overline{B}+C\right)\cdot\left(\overline{A}+B+C\right)\cdot\left(\overline{A}+\overline{B}+C\right)\cdot\left(\overline{A}+\overline{B}+\overline{C}\right)$

2. A Boolean expression is given below:

$$F = A\cdot B\cdot C + A\cdot\overline{B}\cdot C\cdot D + A\cdot\overline{C}\cdot D + \overline{A}\cdot B\cdot C\cdot\overline{D} + \overline{A}\cdot B\cdot C\cdot D$$

   i. Use rules of Boolean Algebra to simplify this Boolean function.

   ii. Use Karnaugh map to simplify the Boolean function.

Answer: $F = B\cdot C + A\cdot D$

EG1108 Tutorial 8 (cont.)

3. Use Karnaugh map to simplify the following Boolean function:

$$F = A \cdot B \cdot C + A \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot \overline{C} + \overline{A} \cdot B \cdot \overline{D} + B \cdot \overline{C}$$

Answer: $F = \overline{C} + A \cdot B + B \cdot \overline{D}$

4. From the table shown below, find Z in terms of A, B and C using Product-Of-Sums (POS) form. Use Karnaugh map to simplify the resulting expression.

A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

Answer: $Z = (\overline{A} + \overline{B}) \cdot (\overline{B} + C) \cdot (\overline{A} + C) \cdot (A + B + \overline{C})$

EG1108 Tutorial 8 (cont.)

5. Design a logic circuit to control electrical power to the engine ignition of a speed boat.

   Logic output **I** is to become high if ignition power is to be applied and remain low otherwise. Gasoline fumes in the engine compartment present a serious hazard of explosion. A sensor provides a logic input **F** that is high if fumes are present. Ignition power should not be applied if fumes are present. To help prevent accidents, ignition power should not be applied while the outdrive is in gear. Logic signal **G** is high if the outdrive is in gear and is low otherwise.

   A blower is provided to clear fumes from the engine compartment and is to be operated for five minutes before applying ignition power. Logic signal **B** becomes high after the blower has been in operation for five minutes. Finally, an emergency override signal **E** is provided so that the operator can choose to apply ignition power even if the blower has not operated for five minutes and if the outdrive is in gear, but not if gasoline fumes are present.

   i. Prepare a truth table listing all combinations of the input signals **B, E, F** and **G.** Also show the desired output **I** for each row in the table.

   ii. Using the sum-of-products approach, write a Boolean expression for **I.**

   iii. Minimize this expression using Karnaugh map. Answer: $\mathbf{I} = \mathbf{E} \cdot \overline{\mathbf{F}} + \mathbf{B} \cdot \overline{\mathbf{F}} \cdot \overline{\mathbf{G}}$

   iv. Implement the logic circuit with the least number of gates (you can assume that AND, OR and NOT gates are available).